CLAIMS

1. (Previously presented) A video processing circuit, comprising:

a processor operable to:

receive a signal including an overlay frame and an encoded image frame having first and second regions;

decode the overlay frame and the first region of the image frame;

modify the decoded first region of the image frame to include the decoded overlay frame; and

re-encode the modified first region of the image frame;

where the overlay frame is distinct from the encoded image frame including the first and second regions in the signal.

2. (Previously presented) The video processing circuit of claim 1 wherein the processor is operable to combine the encoded second region of the image frame and the re-encoded first region of the image frame to generate an encoded modified image frame.

3. (Original) The video processing circuit of claim 1 wherein the processor is operable to:

decode the first region into a transform domain; and

modify the decoded first region in the transform domain.

4. (Original) The video processing circuit of claim 1 wherein the processor is operable to:

decode the first region into a pixel domain; and

modify the decoded first region in the pixel domain.

5. (Previously presented) The video processing circuit of claim 1 wherein:

the first region has dimensions and a location within the image frame; and

the processor is operable to receive the dimensions and location of the first region within the image frame.

6.-37. (Canceled)

38. (Previously presented) A method, comprising:

receiving a video signal including an encoded image frame and an overlay frame;

decoding a first region of the encoded image having the first region and a second region;

decoding the overlay frame;

in response to an overlay command, modifying the decoded first region to include the decoded overlay frame; and

re-encoding the modified first region;

where the overlay frame is distinct from the encoded image frame including the first and second regions in the signal.

39. (Previously presented) The method of claim 38, further comprising combining the encoded second region of the image frame and the re-encoded first region of the image to form an encoded modified image frame.

40. (Original) The method of claim 38 wherein:

the decoding comprises decoding first region into a transform domain; and

the modifying comprises modifying the decoded first region in the transform domain.

41. (Original) The method of claim 38 wherein:

the decoding comprises decoding the first region into a pixel domain; and

the modifying comprises modifying the decoded first region in the pixel domain.

42.-64. (Canceled)

65. (Previously presented) The video processing circuit of claim 1 wherein the processor is operable to:

store the re-encoded modified first region and the second region.

66. (Previously presented) The video processing circuit of claim 65 comprising a buffer to store the re-encoded modified first region and the second region.

67. (Previously presented) The video processing circuit of claim 65 wherein the processor is operable to decode the first region of the image and the overlay frame by identifying motion vectors.

68. (Previously presented) The method of claim 38 comprising storing the re-encoded modified first region and the second region.

69. (Previously presented) The method of claim 38 including re-encoding the modified first region responsive to rate controlling.